AMENDMENT TO THE SPECIFICATION

Please replace the paragraph appearing on page 14, lines 1-16 with the following amended paragraph:

FIG. 2 is a functional block diagram of the read command return portion of a slave device 12 containing a split command look-ahead apparatus 13 in accordance with the present invention. Slave device 12 is associated with a peripheral device 50, such as an external memory, and its associated device controller 52. FIFO 54 is a first-in, first out (FIFO) data register receives data returned from the peripheral device 50 for transfer to the requesting master device via bus 34. Device controller 52 returns the command to the read return portion of the slave device. The returned command includes the master ID in the form that appears on line 26 (i.e., HMASTER). The master ID is returned to a return register in the form of a command queue FIFO 56 at the same time that the last beat of data is returned to data FIFO 54.

Please replace the paragraph appearing on page 15, lines 5-12 with the following amended paragraph:

Return decoder 62 is a control device, which is responsive to the master ID in register 58 and to a HMASTER code on line 26 from arbiter 14 to indicate a match. If the code in register 58 matches the HMASTER code on line 26, decoder 62 provides a MAST_MATCH signal to FIFO 56 causing FIFO 56 to issue the next command master ID to register 58 and to decrement the count in counter 60.

Please replace the paragraph appearing on page 15, lines 13-25 with the following amended paragraph:

~~Read~~Return decoder 62 includes a single-bit validity

register 64 that identifies the validity of the command master ID in register 58. The validity bit is set when a master ID is written into staging register 58 from FIFO 56 and is reset (invalidated) when a match is found by decoder 62 between the HMASTER code on line 26 and the master ID code in register 58. FIFO 56 operates to insert the next master ID into staging register 58 whenever the validity bit indicates an invalid master ID in the staging register (e.g., the validity bit is low). If no command master ID is present in FIFO 56 (i.e., if FIFO 56 is empty), the validity bit remains low.